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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/714,001	11/14/2003	Tzu-Ching Tsai	10113201	1528

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EXAMINER	
PHAM, THANHHA S	
ART UNIT	PAPER NUMBER
2813	

DATE MAILED: 09/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

Office Action Summary	Application No.	Applicant(s)	
	10/714,001	TSAI ET AL.	
	Examiner	Art Unit	
	Thanhha Pham	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 July 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *12-20* is/are allowed.

6)☒ Claim(s) *1,5-8,10 and 11* is/are rejected.

7)☒ Claim(s) *2-4 and 9* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to Applicant's Amendment dated 07/05/2005.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

1. **Claims 1 and 6-7 are rejected under 35 U.S.C. 102(e) as being anticipated by Kitamura [US 6,815,752].**

► With respect to claim 1, Kitamura. (figs.5-31, cols. 1-14) discloses a method of forming a bit line contact via, comprising:

providing a substrate (50, fig. 5, col. 8 lines 46-67) with a transistor thereon, the transistor having a gate electrode (10), drain region (14), and source region (13);

forming a conductive layer (32', fig. 5, col. 8 lines 46-67) overlying the drain region (14), wherein the top surface of the conductive layer is lower than that of the gate electrode;

conformally forming an insulating barrier layer (15, fig. 5, col. 9 lines 1-3) overlying the substrate (50);

blanketly forming a dielectric layer (16, fig. 6, col. 9 lines 4-10) overlying the insulating barrier layer (15); and

forming a via (18a, fig. 6, col. 9 lines 4-10) through the dielectric layer (16) and the insulating barrier layer (15), exposing the conductive layer (32').

► With respect to claim 6, Kitamura (fig.5, col. 9 lines 1-3) discloses that the insulating barrier layer (28) comprises SiN.

► With respect to claim 7, Kitamura (fig.6, col. 9 lines 4-10) discloses that the dielectric layer (16) comprises an oxide.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kitamura [US 6,815,752] in view of Koubuchi et al. [US 6,664,642].

Kitamura substantially disclose the claimed method except teaching that the dielectric layer comprises boro-phosphosilicate glass (BPSG). However, Koubuchi et al. discloses that the dielectric layer (36) can be a silicon oxide or BPSG (fig. 19, col. 20 lines 34-48). Therefore, it would have been obvious to one of ordinary skill in the art at to select either silicon oxide or BPSG for the dielectric layer in the Kitamura because, as taught by Koubuchi et al., such materials are equivalence for their use in the

semiconductor art as the insulating dielectric materials (see col. 20, lines 46-48). Moreover, selection of a known material based on its suitability for its intended use supported a prima facie obviousness determination in Sinclair & Carroll Co., Inc. v. Interchemical Corp., 325 U.S. 327, 65 USPQ 297 (1945).

3. Claims 1 and 5-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Amo et al [US 6,690,052] in view of Rhodes [US 6,458,651].

► With respect to claim 1, Amo et al. (figs.1-5, cols. 5-8) discloses a method of forming a bit line contact via, comprising:

providing a substrate (1, fig. 2, col. 6 lines 6-17) with a transistor thereon, the transistor having a gate electrode (7), drain region (12), and source region (12);

forming a conductive layer (19, fig. 4, col. 8 lines 1-3) overlying the drain region (12);

conformally forming an insulating barrier layer (28, fig. 4, col. 8 lines 7-10) overlying the substrate (1);

blanketly forming a dielectric layer (29, fig. 4, col. 8 lines 11-14) overlying the insulating barrier layer (28); and

forming a via (42, fig. 5, col. 8 lines 24-44) through the dielectric layer (29) and the insulating barrier layer (28), exposing the conductive layer (19).

Amo et al teaches using the conductive layer (19) for bitline contact but does not teach the top surface of the conductive layer (19) is lower than that of the gate electrode.

However, using the conductive layer with the top surface being lower than that of the gate electrode for bit line contact has been known in the art. See Rohdes (figs 2 & 6, cols. 3-6) as an evidence that shows using the conductive layer (34, figs 2 & 6) with the top surface being lower than that of gate electrode (17 or 18) for bit line contact to the drain region (22). Rhodes also mentions that the conductive layer being used for bit line contact can have the top surface being either lower or higher than that of the gate electrode (col. 3 lines 60-67).

Therefore, at the time of invention, it would have been obvious for those skilled in the art modify process of Amo et al by using the conductive layer with the top surface being lower than that of the gate electrode as taught by Rhodes to provide a protection to the drain of the transistor when forming the contact hole for bit line contact.

► With respect to claim 5, Amo et al. (fig.4, col. 8 lines 1-3) discloses that the conductive layer (19) is doped polycrystalline silicon.

► With respect to claim 6, Amo et al. (fig.4, col. 8 lines 8-9) discloses that the insulating barrier layer (28) comprises SiN.

► With respect to claim 7, Amo et al. (fig.4, col. 8 lines 11-12) discloses that the dielectric layer (29) comprises an oxide.

► With respect to claim 8, BPSG is a known silicon oxide for dielectric layer in forming bit line contact via of semiconductor. Selection of a known material based on its suitability for its intended use supported a prima facie obviousness determination in Sinclair & Carroll Co. v. Interchemical Corp., 325 U.S. 327, 65 USPQ 297 (1945) "Reading a list and selecting a known compound to meet known requirements is no

more ingenious than selecting the last piece to put in the last opening in a jig-saw puzzle." 325 U.S. at 335, 65 USPQ at 301. See also In re Leshin, 227 F.2d 197, 125 USPQ 416 (CCPA 1960) (selection of a known plastic to make a container of a type made of plastics prior to the invention was held to be obvious). See Rhodes (fig 2, col 4) as an evidence that shows using BPSG for the dielectric layer in the process of forming the bit line contact via. Therefore, at the time of invention, it would have been obvious for those skilled in the art, in view of Rhodes, to use BPSG as the known material as being claimed in the process of Amo et al to define bit line contact area to the drain region of semiconductor device.

4. Claims 10-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Amo et al. [US 6,690,053] in view of Rhodes [US 6,458,651] as applied to claim 5 above, in further view of Saito et al. [US 6,399,438].

Amo et al. in view of Rhodes substantially discloses the claimed method except teaching that the polycrystalline silicon is doped with As. However, Saito et al. discloses that the polysilicon (21) is doped with As (col. 16 lines 53-56). Therefore, at the time of invention, it would have obvious for those skilled in the art to modify process of Amo et al. by using polyscrystalline silicon doped with As in the conductive layer as taught by Saito et al. to increase the conductivity of the conductive layer.

Allowable Subject Matter

5. Claims 12- 20 are allowed.

6. Claims 2-4 and 9 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

7. The following is a statement of reasons for the indication of allowable subject matter:

► Recorded Prior Art fails to disclose the combination of the process steps of forming a bit line contact via as cited in the base claims 12 and 20 including: removing the unwanted conductive layer and doped polycrystalline silicon layer, leaving the doped polycrystalline layer thinner than the gate electrode, overlying the drain region, and the conductive layer covered by the doped polycrystalline silicon layer; conformally forming an insulating barrier layer overlying the substrate; blanketly forming a dielectric layer overlying the insulating barrier layer; and forming a via through the dielectric layer and insulating barrier layer, exposing the doped polycrystalline silicon layer.

► Recorded Prior Art fails to disclose the combination of the process steps of forming a bit line contact via as cited in the base claim 1 wherein forming the conductive layer further comprising: blanketly forming a layer of conductive material overlying the substrate; removing a portion of the conductive material layer, leaving a conductive layer overlying the drain region and source region wherein the top surface of the conductive layer is lower than that of the gate electrode; forming a patterned resist layer exposing the conductive layer overlying the source region; removing the exposed conductive layer using the patterned resist layer as a mask; and removing/ashing the patterned resist layer as characteristics in claims 2, 3 or 4.

Response to Arguments

8. Applicant's arguments with respect to claims 1, 5-8 and 10-11 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

9. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanhha Pham whose telephone number is (571) 272-1696. The examiner can normally be reached on Monday and Thursday 9:00AM - 9:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead can be reached on (571) 272-1702. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Thanhha Pham
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Patent Examining Group 2800

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PRIMARY EXAMINER